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(54) **Differential bus drivers.**

(57) This invention relates to differential bus drivers for use in, for example, communication systems. The driver achieves highly symmetrical wave forms at the output stage for both high and low side drivers. In addition, the layout of components of the high and low side drivers is substantially identical which allows production of the driver as an integrated circuit with a simple layout.

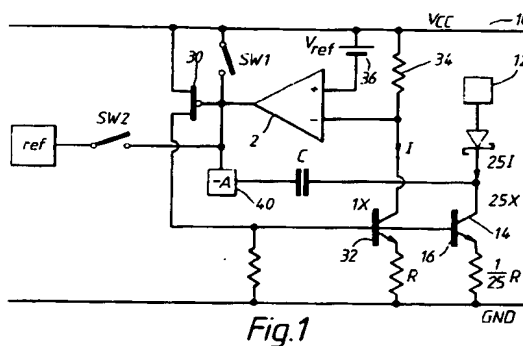


Fig.1

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This invention relates to Differential Bus Drivers for use in, for example, electronic communications systems.

In electronic communication systems such as, for example, Automotive multiplex wiring, computer interfaces, etc, there are often one or more data buses connecting subcircuits of the system. In order for a signal to be transmitted from the data buses to either internal or external subcircuits of the system, Bus drivers are generally utilised. One such type of Bus driver circuit is a Differential bus Driver.

Differential bus drivers are generally incapable of producing symmetrical outputs when operating with both current sink and current source capabilities. In addition, the circuitry required to facilitate the two types of capabilities is often fairly complex in layout and design.

Accordingly one object of the present invention is to provide a differential bus driver which achieves highly symmetrical wave forms.

Another object of the invention is to provide a differential bus driver which is as applicable to voltage mode interface standards such as RS422, Controller Area Network (CAN), Automotive Multiplex Wiring System (Abus) as it is to current mode standards like Vehicle Area Network (VAN).

According to one aspect of the present invention, there is provided a differential bus driver having a low side driver circuit and a high side driver circuit, said circuits both having substantial identical AC and DC characteristics wherein each circuit comprises an amplifier configured to monitor output of the driver circuit and maintain said output at a predetermined value, a first semiconductor device adapted to produce the output and a second semiconductor device capable of driving the first semiconductor device in response to a signal generated by said amplifier.

This has the advantage of providing highly symmetrical output stages since the devices are matched on the same Integrated Circuit. In addition, the layout of the driver is greatly simplified due to the symmetrical design.

Preferably the driver further comprises a third semiconductor device forming a current mirroring device with the first semiconductor device, such that the amplifier monitors a characteristic of the third semiconductor device in order to monitor and maintain said output.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a low side driver according to the present invention;

Figure 2 is a circuit diagram of a high side driver according to the invention; and

Figure 3 is a circuit diagram of a preconditioning circuit for the driver of Figure 1 or Figure 2.

The circuits of Figure 1 and 2 show respectively an output driver with current sink capability (low side

driver) and output driver with current source capability (high side driver). These circuits are under current mode control. The aim of the illustrated circuits is to illustrate a current source which has identical AC and DC characteristics to a matching current sink. This is achieved by using a feedback system to control how the currents are generated. The circuits allow the use of the same amplifier scheme 2 in both the source and the sink circuit. This is possible due to the fact that in both circuits the current in the output is measured with respect to the positive rail Vcc. In one circuit 10 (the current sink) the output 12 is taken from the collector 14 of an NPN 16 and in the other circuit 18 (the current source) it is taken from the Emitter 20. Diodes are included to allow the outputs to be of high impedance to the output rail voltages. Because both circuits use a matched PMOS 30, amplifier 2 and NPN 16 the propagation delay also is well matched. The propagation delay when the circuit is turned on can be further enhanced by forcing the gate voltage to a point which is dependent on process parameters of the NPN and PMOS using SW2. Such a reference can be made as in circuit 3. The output is turned on and off by respectively opening and closing SW1. SW1 and SW2 may be implemented using MOS switches.

The circuits can be adapted for use in voltage mode control in the following manner.

Slow rate can be controlled by the addition of a Capacitor C and the use of a current mirror to invert the current signal in the case of the low side. As $I=C(dv/dt)$ if the current provided into the capacitor is controlled a controlled slew can be achieved.

The high and low side drivers will now be described in greater detail.

Both high side and low side drivers use the same components. An output NPN 16 is configured in either common collector mode (Figure 2) or in common emitter mode (Figure 1). The output stage current is monitored by a current mirror configured NPN 32 connected to the output NPN. To sense the current only a small proportion of the output stage current, for example, 1/50th is fed through the current mirror. For the high side driver, this current adds to the output stage, but can be compensated for and forms only a small error.

The current in the output leg of the current mirror is converted to a voltage signal by means of a precision resistor 34, made of a material which matches to the current defining element (current reference circuit) elsewhere in the circuit. A high speed transconductance amplifier 2 then measures the voltage across the sense resistor, the amplifier differential input being referenced to a precision voltage reference 36. Thus the desired current setting can be defined either by an internal voltage source, or by an external current source. An external current source can be an inherently more precise scheme since the absolute value of current defining resistors on an IC is difficult

to define precisely.

In both circuits, the output NPN is driven by a PMOS transistor 30. The transconductance amplifier output drives the gate of the PMOS device. In operation, the amplifier is allowed to drive the gate of the PMOS such that the NPN delivers output current up to the limit determined by the feedback loop thus formed. Thus the output stages are current limited. To set the system frequency response, a capacitor can be added to the gate of the PMOS (which is already capacitive) and the transconductance (G_m) of the transconductance amplifier is programmed (e.g. by means of a resistor).

If desired the feedback to the PMOS gate may also be influenced by the voltage on the driver output. For example, capacitive feedback from the output to the gate of the PMOS can cause the output voltage swing to the slow rate controlled. The polarity of the feedback must be adjusted depending upon the polarity of the output, i.e. depending upon whether it is high side or low side. This may be achieved using an inverter 40.

Also, to control the DC output voltage swing, DC voltage feedback loops (not shown) can also be formed. This can, for example, be made to limit the saturation of the NPN output stage (in the low side driver).

It is desired in one application of the driver that the output stages be primarily current controlled, and thus should present a high impedance current characteristic independent of the output voltage.

For the low side driver, this is achieved by relying upon the high output impedance characteristics of conventional Integrated Circuit NPN transistors which typically have an "early voltage" of near 100V. The PMOS VDS voltage in this case remains constant, and hence the G_m characteristics of this device are not varied as the output voltage moves.

However, for the high side driver, this is not the case. The NPN as before has an inherently high output impedance, but as the output voltage moves, so does the PMOS VDS voltage.

This causes a dynamic change to the DC and AC characteristics of the feedback loop. The application of a very high speed transconductance amplifier largely eliminates these effects except at the extreme point as the PMOS VDS collapses to near zero.

The application of these drivers requires the dynamic current and voltage behaviour of the two output stages to be as symmetrical as possible. At the point of initial turn on, the low side driver output voltage is typically at say 5V ($V_{supply}=5V$). For the high side driver, the output voltage is zero. Thus at the point of turn ON the VDS voltages for the two PMOS devices are almost identical. A preconditioning circuit (a scheme of which is shown in Figure 3 and described in more detail below) defines an "ideal" aiming voltage that the PMOS gate should be at in order to gen-

erate the required current on the output stage, and is approximately the same VDS for either high or low side drivers.

At the point of turn on, this voltage is impressed upon the output of the transconductance amplifier, to provide a rapid turn on from zero output current to maximum output current.

Typically, the output drivers would be loaded by a passive cable having a resistive and capacitive load; as the driver stages turn on, thus the output voltages change according to the current generated and the load impedance characteristics (Ohm's law applies).

If this is primarily capacitive the constant current driver output stages cause a linear increase in output voltage over time. Thus for the high side driver, the PMOS VDS changes. The feedback loop frequency response is optimised such that the loop speed is relatively fast compared to the required transition speed of the output voltage waveform. Thus the changing VDS of the high side PMOS has little impact upon the eventual current and voltage wave forms generated.

Referring to the preconditioning circuit, this can be designed in many ways. One preferred embodiment of the circuit 50 is shown in Figure 3. The circuit comprises a current source 52 which generates a current that after processing is output via switch 54 to the PMOS 30 in Figures 1 and 2. The circuit 50 further includes a PMOS 56, an NPN transistor 58 and three PNP transistors 60, 62, 64 and a resistor 66. Transistors 64 has a rectifying function whilst the other components all form part of a feedback loop which controls the V_{be} on transistor 64.

The high side and low side drivers schemes can be generated from identical circuits, simply changing the output node connections. Various blocking diodes may be required and these would be replicated for both types of driver to ensure the same parasitics apply. Similar considerations can be applied to any other specific circuit modifications required for either high or low side driver.

Since both circuits are essentially the same, identical structures and whole cells they can be implemented on an integrated circuit. The identical circuits, scheme of operation and matching layouts all help to ensure the eventual output wave forms are as symmetrical as possible.

Voltage mode standards provide control over the wave shapes by limiting the maximum dv/dt and in current mode systems the outputs act like current sources and sinks and the wave forms are then controlled by the line impedance.

Claims

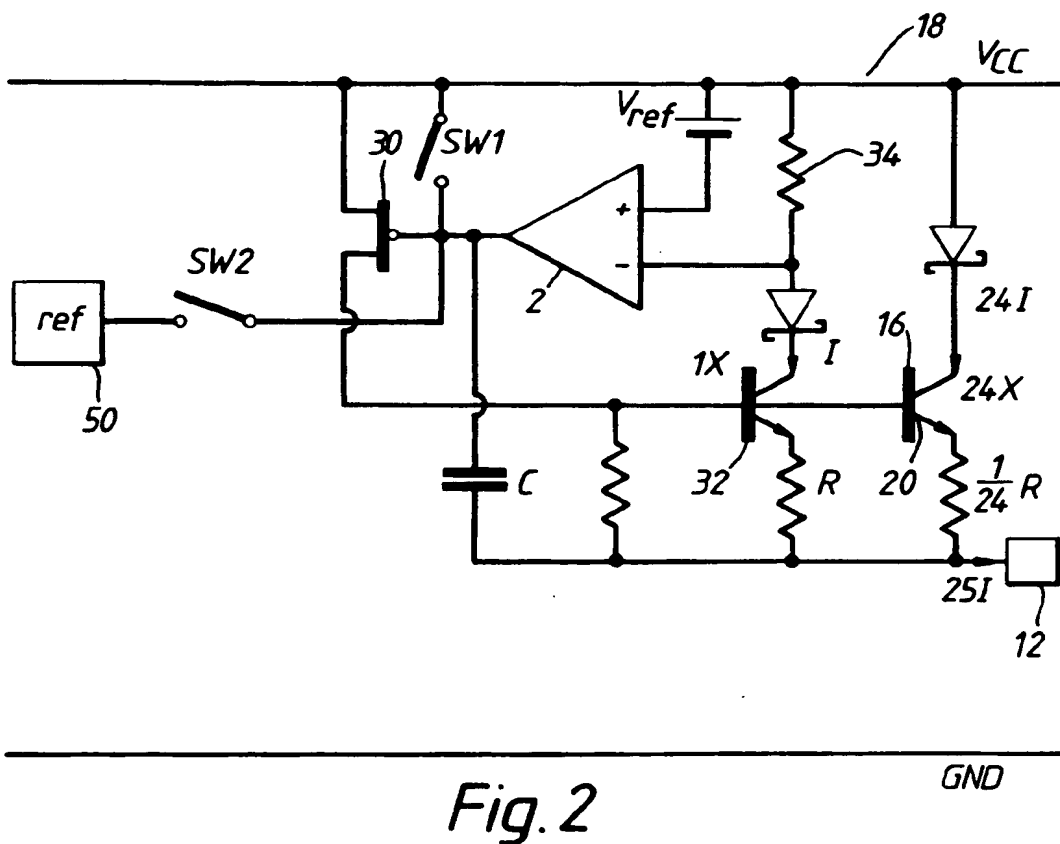
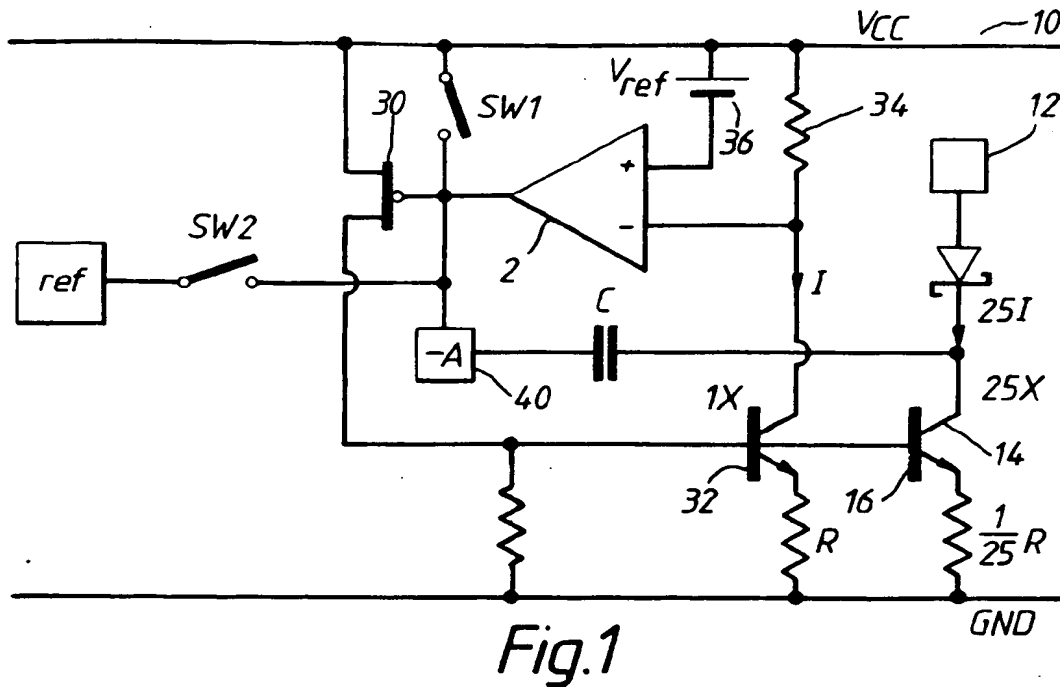
1. A differential bus driver having a low side driver circuit and a high side driver circuit, said circuits

both having substantial identical AC and DC characteristics wherein each circuit comprises an amplifier configured to monitor output of the driver circuit and maintain said output at a predetermined value, a first semiconductor device adapted to produce the output and a second semiconductor device capable of driving the first semiconductor device in response to a signal generated by said amplifier.

2. A differential bus driver according to claim 1, wherein the driver further comprises a third semiconductor device forming a current mirroring device with the first semiconductor device, such that the amplifier monitors a characteristic of the third semiconductor device in order to monitor and maintain said output 15
3. A differential bus driver according to claim 2, wherein the characteristic monitored is collector current. 20
4. A differential bus driver according to claim 2, wherein the characteristic monitored is collector voltage. 25
5. A differential bus driver according to any of claims 2 to 4, wherein the third semiconductor device is an NPN transistor. 30
6. A differential bus driver according to any preceding claim further comprising a preconditioning circuit which defines an operating characteristic of the second semiconductor device to enable relatively fast operation of the driver. 35
7. A differential bus driver according to any preceding claim, wherein the second semiconductor device is a PMOS. 40
8. A differential bus driver according to any preceding claim, wherein the first semiconductor devices are NPN transistors.
9. A differential bus driver according to any preceding claim, wherein the first semiconductor device of the low side driver circuit is an NPN transistor configured in common emitter mode. 45
10. A differential bus driver according to any preceding claim, wherein the first semiconductor device of the high side driver circuit is an NPN transistor configured in common collector mode. 50
11. A differential bus driver according to any preceding claim, wherein both the high and low side driver circuits are fabricated on a single integrated circuit. 55

12. A differential bus driver according to claim 11, wherein the circuit layout for both the high and low side drivers are substantially identical.

- 5 13. A differential bus driver according to any preceding claim, wherein the driver functions in a voltage mode.
- 10 14. A differential bus driver according to any of claims 1 to 12, wherein the driver functions in a current mode.



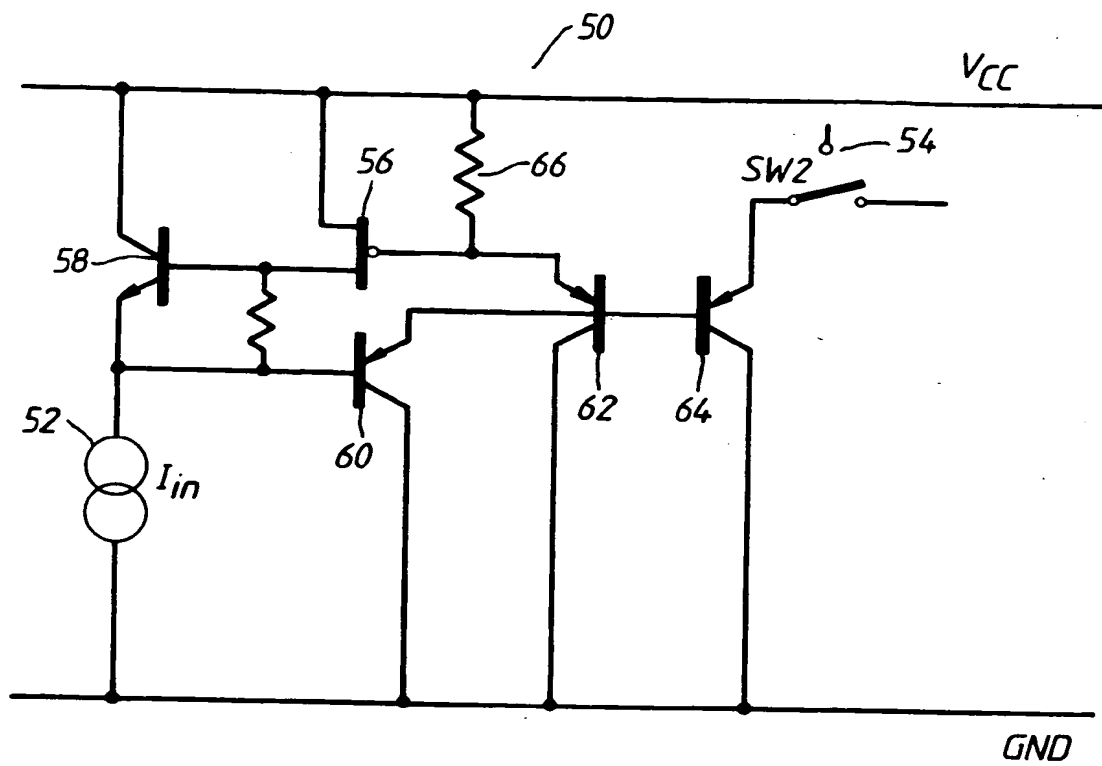


Fig. 3



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 94 30 0843

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CLS)
A	US-A-4 959 561 (MCDERMOTT ET AL.) * column 2, line 43 - column 3, line 42; figure 1 *	1-14	H03K19/003 G06F13/40
A	EP-A-0 102 110 (N. V. PHILIPS' GLOEILAMPENFABRIEKEN) * page 3, line 6 - page 8, line 2; figure 1 *	1	
			TECHNICAL FIELDS SEARCHED (Int.CLS)
			H03K G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 6 June 1994	Examiner Jones, H
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